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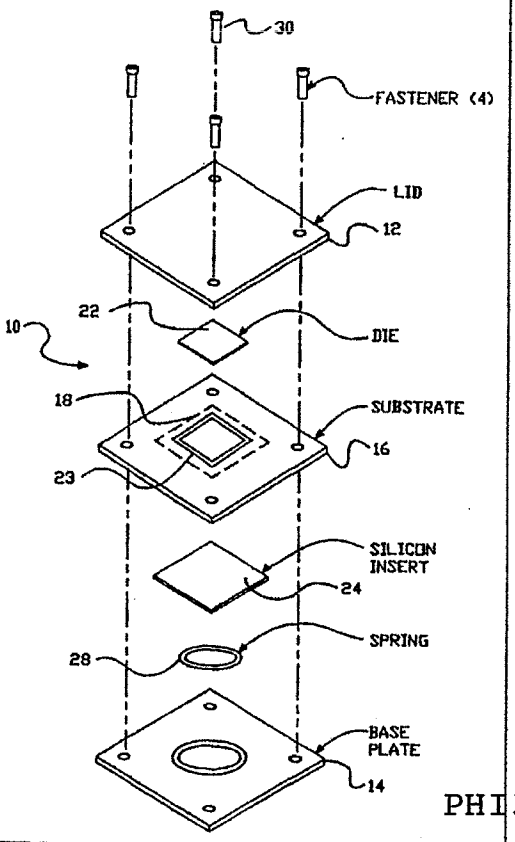
(57) Abstract

A semiconductor die carrier (10) is provided for testing semiconductor circuits, the carrier (10), containing: a substrate (16) defining an opening and an outer perimeter (16); I/O pads (18) about the perimeter and an interconnect circuit (37) which includes individual electrical conductors formed in a polymer dielectric. The interconnect circuit overlays a top surface of the substrate and extends across the opening to form a flexible membrane (20) that spans the opening. Die contact pads connected to the conductors are disposed about the membrane with particles deposited on the die contact pads. A fence (23) upstanding from the membrane (20) and sized to receive a test die (22); a top cap (12) that rests upon the die when the die is received within the fence, a bottom cap (14) that rests against a bottom surface of the substrate; and a fastener (30) for securing the top cap to the bottom cap with the die in between are also provided.



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DIE CARRIER AND TEST SOCKET FOR LEADLESS SEMICONDUCTOR DIE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates generally to the testing of semiconductor circuits and more particularly, to die carriers used to make electrical contact with the pads of a bare semiconductor circuit die during functional and burn-in testing.

2. Description of the Related Art

A major challenge in the production of multichip modules is the identification of defective integrated circuit chips. The yield rate of multichip modules can be significantly increased through the use of fully tested and burned-in die. The testing of die prior to packaging or assembly into multichip modules reduces the amount of rework which in turn decreases manufacturing costs.

Functional tests determine whether a semiconductor circuit operates in accordance with prescribed specifications. Burn-in tests identify latent or inherent manufacturing defects caused by factors like contamination or process variations

during manufacture. Such defects can cause early failure. Burn-in tests subject the die to electrical stress at high power supply voltages with increased temperatures so as to accelerate such early failure to the point of detection.

One problem with the testing of bare die is that as circuit dimensions have become smaller, so have the pads on the die surfaces. Moreover, these smaller pads often are packed more closely together. As a result, it sometimes can be impractical to use devices such as probe cards to make electrical contact with die pads for testing purposes. Another problem with probe cards has been their relatively poor performance in testing high frequency signals.

Some of the shortcomings of probe cards have been overcome through the use of temporary die carriers. For example, gold can be applied to the contact pads of a die, and the die can be placed in a temporary carrier in which it is held in electrical contact with gold pads on the carrier through the application of pressure to the pad-to-pad interface. The use of gold, however, can be too expensive for many semiconductor processes. Another approach is to wire bond the die pads to an intermediate test package. Although the die can be removed from the package after testing by removal of the wire bonds, this can result in damage to the circuit. Consequently, some manufacturers include both the die and its intermediate test package in

the final IC package in order to reduce the possibility of such damage.

Still another approach is disclosed in U.S. Patent No. 5,123,850 issued to Elder et al which teaches the use of an interconnect circuit formed in a resilient membrane to make temporary electrical contact with pads disposed on a die. The interconnect circuit is formed from alternating layers of polyimide dielectric and metal signal lines. Electrical contact bumps protrude from a top surface of the membrane and make electrical contact with individual signal lines. A semiconductor die is placed on the membrane and is aligned by visible means to ensure that the contact bumps are disposed opposite pads on the die. An insert plate is placed against a bottom surface of the membrane opposite the die. The interconnect circuit is wire bonded to a pin grid array (PGA) which can be plugged into a test socket base to communicate test signals to and from the carrier. A heat sink is clipped to the PGA, and the die is pressed between the heat sink and the membrane. The force exerted against the die is expected to cause the contact bumps to make electrical contact with the die pads.

While earlier carriers such as the one described above contain good design concepts there have been shortcomings with their use. For example, the gold coated bumps on the contact pads often do not make adequate contact with the die pads because of the build-up of an oxide layer on the die pads.

In addition, the use of visual means to align the die with the flexible membrane can be somewhat clumsy and time consuming or may require elaborate vision and robotic systems. The use of wire bonding and the use of a PGA can be expensive. The wire bonding of the interconnect circuit to the PGA can make it difficult to interchange one interconnect circuit configured to test one type of die with another interconnect circuit configured to test another type of die. Furthermore, using the heat sink cavity to hold the die aligned to the membrane can be impractical and expensive.

Thus, there has been a need for an improved carrier for testing bare semiconductor circuit die. There has been a particular need for a carrier in which a flexible interconnect circuit can be easily aligned with the pads of a die. There also has been a need for an improved contact pad structure that can penetrate an oxide layer on the die pads. Furthermore, there has been a need for such a carrier in which test signals can be communicated to and from the carrier without the need to make wire bond connections or to use relatively expensive intermediate circuits such as PGAs to conduct signals to and from the carrier. In addition, there has been a need for a carrier in which one interconnect circuit can be readily interchanged with another interconnect circuit. The present invention meets these needs.

SUMMARY OF THE INVENTION

The present invention provides a new bare die carrier for use in testing semiconductor circuits. In a present embodiment, the carrier includes easily accessible I/O pads for conducting test signals to and from the carrier. This carrier has a fence that upstands from a flexible membrane and can be used to align the die with the interconnect circuit. It also includes a mechanism for adjusting the force with which the die is pressed against the interconnect circuit in order to ensure adequate electrical contact without causing damage.

A current implementation of the carrier includes a flexible interconnect circuit which overlays a top surface of a rigid substrate. The substrate defines an opening surrounded by a perimeter region. The interconnect circuit extends across the center opening so as to form a flexible membrane that spans the opening. A multiplicity of I/O pads are disposed about the perimeter of the substrate. Individual electrical conductors of the interconnect circuit are connected to individual I/O pads so as to form a multiplicity of individual electrical paths between the I/O pads and selected locations of the interconnect circuit where die contact pads are formed. A fence upstands from the interconnect circuit and is sized to receive a test die. A support member abuts against a bottom surface of the circuit. A top cap and a bottom cap are provided. The substrate and the die are secured between the top cap and the bottom cap.

The new carrier provides I/O pads which can be easily reached by circuit probes. There is no need to use expensive intermediate circuitry such as a PGA to communicate test signals with the carrier. The carrier can be easily dropped in a standard burn-in test socket so that the die in the carrier can be tested and burned in. The alignment fence obviates the need to visually align the die with the interconnect circuit. The novel carrier is a general purpose device. It can be used to house dies in a clean protected environment during transport of the die. By simply inserting a different substrate bearing a different interconnect circuit between the top and bottom caps, a different test die circuit design can be housed and tested. There is no need for elaborate steps, such as wire bonding to a PGA, to reconfigure the carrier to test a different type of die.

These and other purposes and advantages of the present invention will become more apparent to those skilled in the art from the following detailed description in conjunction with the appended drawings in which:

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an exploded perspective view of a carrier in accordance with the present invention;

Figure 2 is a top plan view of a substrate/interconnect circuit assembly of the

carrier of Figure 1 showing the interconnect circuit and a fence formed thereon;

Figure 3 is an enlarged cross-sectional view of the substrate/interconnect circuit assembly of the carrier of Figure 1;

Figure 4 is a cross-sectional view along line 4-4 of Figure 3;

Figure 5 is a cross-sectional view of a particle protruding from the contact of Figure 4;

Figure 6 is a cross-sectional diagram representing a fully assembled carrier in accordance with the present invention;

Figure 7A is a cross-sectional view of an alternate substrate/interconnect circuit assembly in accordance with the invention;

Figure 7B is a bottom elevation view of the substrate and support member of the alternate assembly of Figure 7A;

Figure 8 is a side view of an alternate support member and spring member in accordance with the invention;

Figure 9 is a side view of an alternate support member in accordance with the invention;

Figure 10 is a cross-sectional view of an alternate embodiment of the invention which uses alternate means for providing a force to the die/interconnect circuit interface;

Figures 11, 12A, 12B, 13A and 13B show alternate carriers that use different mechanisms for providing a force to the die/interconnect circuit interface in accordance with the invention; and

Figures 14A and 14B show the manner of rotating the top cap into place for the embodiments of Figures 12A-B and 13A-B.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention comprises a novel carrier for use in testing bare semiconductor circuit die. The following description is presented to enable any person skilled in the art to make and use the invention, and is provided in the context of a particular application and its requirements. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the invention. Thus, the present invention is not intended to be limited to the embodiment shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

Referring to the illustrative drawings of Figure 1, there is shown an exploded perspective view of a bare semiconductor circuit die carrier 10 in accordance with the present invention. The carrier 10 includes a top cap 12, a bottom cap 14 and a substrate 16. The substrate 16 has a central opening which extends through it indicated by dashed lines 18 and which is spanned by a flexible membrane 20. The dashed lines 18 also indicate an inner perimeter of the substrate 16. A bare semiconductor circuit die 22 is sized to fit within a fence 23 which upstands from a top surface of the flexible membrane 20. A support 24 abuts against a bottom surface of the membrane 20 within a recess defined by the opening in the substrate 16 indicated by dashed lines 18. The top cap 12 is secured to the bottom cap 14 by fastening mechanisms 30. A spring member 28 is disposed within the recess between the support 24 and the bottom cap 14. The spring member 28 urges the support 24 against the bottom surface of the membrane 20 when the top and bottom caps are fastened together.

Referring to the illustrative drawings of Figure 2, there is shown a top plan view of the substrate/interconnect circuit assembly 37. A polymer dielectric is deposited on both the top and bottom surfaces of substrate 16. An interconnect circuit 32 is formed on the substrate top surface. The interconnect circuit 32 is comprised of a composite of a multiplicity of electrical conductors 34 formed in the polymer. This composite covers the

entire top surface of the substrate and forms the flexible membrane 20 that extends across the opening in the substrate. A multiplicity of input/output (I/O) pads 36 are disposed about the perimeter of the substrate 16. Individual conductors 34 form conductive paths between individual pads 36 and prescribed contact pad locations in the flexible membrane 20. The rectangular fence 23, which upstands from the flexible membrane 20, is sized and contoured such that the semiconductor die 22 will become properly aligned with the interconnect circuit 32 when the die is inserted within the fence.

Thus, the fence is disposed on and upstands from the portion of the interconnect circuit 32 that is surrounded by or circumscribed by the opening 18 through the substrate 16. Consequently, when a test die 22 is placed within the fence, the membrane can flex in cooperation with the support 24 to keep the interconnect circuit 32 planarized for better electrical contact with the die.

It should be understood that, although the conductors 34 of the interconnect circuit 32 of Figure 2 only extend to the edge of the fence 23, an alternative interconnect circuit (not shown) could be employed in which the conductors extended into more central portions of the flexible membrane 20. For example, certain semiconductor circuits use area pads deployed at locations other than the die periphery. In order to test such circuits, the

substrate/interconnect circuit assembly must have conductors that extend further out into the membrane 20 so as to make electrical contact with such area pads.

Furthermore, while the interconnect circuit 32 of Figure 2 has only a single layer of conductors, multiple conductor layers could be used consistent with the invention. The fabrication of a multilevel interconnect circuit 32 is disclosed in U.S. Patent No. 4,812,191 issued to Ho et al. which is expressly incorporated herein by this reference.

In the present embodiment, the substrate 16 is formed from aluminum. However, other substrate materials such as copper, ceramic or silicon could be used. The polymer dielectric is polyimide. Polymer materials with an E value of 2 to 4 are particularly useful in this application. The interconnect conductors 34 are formed from copper, but other conductive materials such as aluminum could be employed.

During manufacture of the substrate/interconnect circuit assembly, the center opening is formed in the substrate and the polymer layer formed on the substrate. The top surface of the substrate 16 is first coated with pressure sensitive tape or photoresist, or possibly both, to provide mechanical and chemical protection for the electrical circuitry. A recess is then mechanically machined into the bottom surface of the substrate 16 through

the polymer and into the aluminum. The recess is machined about 80% of the way through the substrate. For a 50 mil substrate, for example, the recess will be about 40 mils deep. The area of the recess will correspond to the size of the flexible membrane to be formed. Several recesses can be machined into a single large substrate to form multiple membranes, or single large recess can be machined, making one large membrane.

Any number of methods can be used to machine the recess. Milling, high-speed routing, EDM (electrostatic discharge machining), beadblasting through a mask can all be used, depending upon precision and cost constraints.

The recessed substrate is now chemically etched to remove the remaining 20% of the substrate thickness left in the bottom of the pocket, leaving intact the flexible membrane which spans the newly formed opening in the substrate. The bottom of the substrate is protected from the etchant by the backside polymer layer which forms a mask. Since the 20% remaining thickness of the substrate in the recess is thin relative to the thickness of the substrate in the recess area, little undercut occurs, even with an isotropic etchant.

Any number of etchants can be used as long as the insulating material used in forming the electrical circuits on the substrate is not chemically attacked by it. The etchant temperature

must be carefully controlled to provide a constant etch rate. This is essential to controlling the tensile stress in the interconnect circuit. The protective layers on the top of the substrate are now removed.

The removal of the substrate from beneath a portion of the interconnect circuit leaves the flexible membrane 20 which spans the opening and defines the recess in the bottom surface of the substrate/interconnect circuit assembly in which the support member 24 is placed. In the current embodiment, the support member is formed from silicon so as to match the coefficient of thermal expansion of the silicon die under test. A top surface of the support member can have a polymer layer such as polyimide deposited on it to provide more compliance to the contact pads on the circuit.

Referring to the illustrative drawing of Figure 3, there is shown a cross-sectional view of a portion of the substrate/interconnect circuit assembly 37. A polyimide dielectric layer 39 has an electrical conductor 34 formed on it. The conductor 34 makes a connection with a contact pad 40 exposed on a top surface of the membrane 20. Portions of the top layer conductors are exposed; however, other conductors (not shown) can be buried in the polymer 39. In some cases multiple conductor layers are required to route signals. For example, Figure 4 shows conductor traces 34 buried in the polymer, and Figure 3 shows conductor traces partially exposed on

top of the polymer and partially protected (covered) by the fence 23. The exposed contact pad 40 must be aligned with a corresponding pad 45 on the surface of the test die 22 in order for the conductor 34 to be able to form an electrical path between the die pad 45 and one of the I/O pads 36. The fence 23 is formed from a thicker polymer layer which overlays and protects the conductor 34. The fence is circumscribed or surrounded by the opening 18 formed in the substrate 16, and it extends outward to the I/O pad 36.

Referring to the illustrative drawings of Figure 4, there is shown a cross sectional view along line 4-4 in Figure 3. The conductor 34 is formed in the polymer layer 39. An electrical contact pad 40 is exposed on a top surface of the polymer layer 39 and is in electrical contact with conductor 34 via conductive path 42. A number of hard conductive particles 44 protrude from a top surface of the contact pad 40. An aluminum die pad 45 formed on a surface of the die 22 is aligned with electrical contact pad 40. As more fully described below, the particles 44 penetrate any impurity such as an oxide layer which may have formed on the surface of the aluminum die pad 45.

Referring to the illustrative drawing of Figure 5, there is shown a somewhat enlarged cross sectional view of one of the particles 44 of Figure 4. In the present embodiment, the particle is both mechanically hard and electrically conductive. The

particle 44 is embedded in a layer of a hard metal 46 (such as nickel or tungsten) which binds the particle to the contact pad 40. A layer of nonoxidizing metal 48 such as gold is deposited on the particle. The purpose of the gold layer is to keep the contact pad 40 from oxidizing and to facilitate electrical contact between the contact pad 40 and the die pad 45. Alternatively, nonconductive particles can be used if they are covered with an appropriate conductive material and have a hardness greater than the metal of the die pad 45.

Using partical plated contact pads obviates the need to devise elaborate mechanical schemes to generate a wiping action to push aside any oxide layer on pad 45. Instead, electrical contact is made by the particles penetrating through the oxide layer on pad 45 with a simple normal force.

The flexibility of the interconnect circuit membrane contributes to the achievement of electrical contact between each of the contact pads 40 and the die pads 45 for the following additional reasons. In practice, some contact pads 40 protrude upwards further from the interconnect circuit top surface than others. This is the result of typical manufacturing variations within prescribed tolerances. In order to ensure proper electrical contact with all such contact pads 40, however, it is necessary to equalize their height displacement. That is, it is necessary to planarize or level the

pads 40 with respect to each other. Since the circuit membrane is compliant, a normal force applied by the properly aligned die 22 can push down those pads 40 that stand up too far so that all of the pads 40 are planarized. The compliance of the circuit membrane permits the pads 40 that jut upwards too far to be pushed downwards so as to be level with the other pads.

The purpose of the opening 18 is to afford additional compliance to the circuit 32. As an alernative, instead of providing an opening, the polymer dielectric of the fenced-in portion of the interconnect circuit could be made sufficiently thick to provide the desired degree of compliance. For example, it has been found that a polyimide layer approximately 36 microns thick can provide sufficient compliance in certain instances. As another alternative, instead of providing the opening, a thinned substrate region beneath the fenced-in portion of the interconnect circuit can provide the required compliance. For example, for a silicon or aluminum substrate, a thinned region approximately 5-10 mils thick can provide sufficient compliance depending upon the height tolerance in the manufacture of the pads 40 of the interconnect circuit. In each of these two alternative embodiments the substrate serves as a support for the interconnect circuit. Thus, the invention is not intended to be limited to a carrier with such a substrate opening.

From the foregoing discussion, it will be appreciated that the correct alignment of the die pads 45 with exposed contacts in the top surface of the membrane 20 is essential to the operation of the carrier. The purpose of the fence 23 is to register the die pads 45 with the exposed pads 40 of the membrane. The fence 23 obviates the need for an elaborate fixturing mechanism to achieve that alignment. The fence can be formed from any of a variety of materials such as, photoimagable polymers, photoimagable metals, mechanical plastics, a metal ring or any combination of these materials. Since the fence is formed by the same processing steps as the contact pads tight tolerances can be obtained for proper alignment operations.

An important consideration is the amount of force that must be applied to the die 22 in order to drive the particles 44 into conductive contact with the die pads 45. As explained above, a conductive coating layer, such as gold which is free of any oxide layer, is deposited on top of the particles 44 which are pressed against the die pad so as to penetrate any oxide layer on the die pad and form an electrical contact. Thus, sufficient force must be applied to drive the particles through any contaminant and to create electrical contact. The amount of force required can vary depending upon the number of pads on the test die. The more pads there are, the more force is required to create electrical contact with all of them.

The carrier of the present invention advantageously permits the application of a controlled amount of force to the die. One mechanism for applying that force will be explained with reference to the drawings of Figure 6 which shows a cross sectional view of an assembled carrier 10. Other possible mechanisms are explained with reference to subsequent drawings. The die 22 is received within a region defined by the fence 23. As explained above, in the present embodiment, the fence is formed from a raised layer of polyimide dielectric which extends from the fence to the outer perimeter of the substrate 16 so as to protect the interconnect circuit 32 from damage while at the same time leaving the I/O pads 36 at the edge of the substrate exposed. The substrate 16 rests upon the bottom cap 14. The top cap 12 abuts directly against the die 22. The top cap is sized so that it overhangs a portion of the interconnect circuit but does not interfere with access to the I/O pads 36. In the present embodiment, the top cap 12 and the bottom cap 14 are formed from a metal. Consequently, the top cap can serve as a heat sink for the die.

A spacer 48 is interposed between the top cap 12 and the substrate/interconnect circuit assembly. In the preferred embodiment, the spacer is made of teflon material. However, other dielectric or metal materials could be used. The purpose of the spacer is to prevent damage to the interconnect circuit 32 and to ensure that the membrane 20 is not

overstressed due to inadvertent application of excessive force. The substrate 16 rests upon the bottom cap 14. The silicon support 24 is disposed within the recess beneath the membrane 20 between the spring member 28 and the membrane 20. The polymer layer formed on the silicon support abuts against the bottom surface of the membrane. The spring member urges the silicon support against the die.

Fasteners 30, shown in Figure 1, are used to attach the top cap to the bottom cap. Spring clips, screws, clamps, rivets or other fastening means, such as those described with reference to Figures 11, 12A-B, 13A-B and 14A-B, could be used. The fasteners could be applied at all four corners of the top and bottom caps 12, 14 or to only two corners of the top and bottom caps 12, 14. The fasteners 30 provide a controlled displacement of the spring member 28. The closer the top and bottom caps are brought together by the fasteners 30, the greater will be the displacement of the silicon support. The silicon support, exerts a uniform and predictable force at the die/membrane interface. The amount of force can be regulated according to how many pads are located on the die. For example, if there are more pads on the die, then the fastening mechanisms would be secured so as to cause a greater displacement of the spring member 28 and a corresponding application of a greater uniform force to the die/substrate interface.

In the present embodiment, the spring member 28 is implemented using a spring which exerts a constant spring force within a certain range of displacement. That is, the spring member 28 applies the same force to the die regardless of variations in the thickness of the die and the carrier components (such as the top and bottom caps) within a prescribed tolerance range. Alternatively, an elastomer could be used as a spring member. As shown in Figure 10, the force can also be applied from the top using the spring(s) 351 in which case the bottom spring is used to planarize the substrate/interconnect circuit assembly against the die. Figures 8 and 9 depict two possible implementations of such insert mechanisms. In Figure 8, a spring or rubber elastomer is used for planarization, and in Figure 9 spherical bearings such as a Torrington Spherical plain angular contact bearing Type SBT produced by Bearings, Inc. is used for planarization.

The polymer layer is formed on the surface of the support 24 with polyimide to provide a small amount of compliance under pressure. The silicon support 24 has a co-efficient of thermal expansion (CTE) which matches that of the silicon die under test. The use of a support with a CTE that matches that of the die helps to ensure that, as the die and the membrane expand at different rates with increased temperature (during burn-in testing for example) that the die pads 22 do not become

misaligned with the exposed contacts 40 in the membrane 20.

Referring to Figures 7A and 7B there is shown a cross-sectional view of an alternate substrate/interconnect assembly 137 and a bottom elevation view of the substrate 116 and support member 124 of the alternate assembly 137. The assembly 137 provides an alternate mechanism to achieve planarization of an interconnect circuit 132 against a test die (not shown). The substrate 116 and the support member 124 are formed from a single semiconductor wafer. A rectangular groove is formed completely through the wafer so as to form a gap 127 that separates the support member 124 from rest of the substrate 116. An inner perimeter of the substrate 116 defines the outer edge of the gap 127. The inner edge of the gap is defined by the support 124. The gap 127 can be formed using processes similar to those used to form the opening 18 in the embodiment first described above. The interconnect circuit spans the gap opening 127 forming a narrow flexible membrane that circumscribes the support member 124.

The interconnect circuit 132 and a fence 123 overlay top surfaces of the substrate 116 and the support member 124. I/O pads 136 are formed about the top perimeter of the assembly 137. Bottom surfaces of the substrate 116 and the support member 124 are placed on to a resilient layer 139 formed from a resilient material such as an elastomer.

The carrier 137 of the alternative embodiment can be secured between top and bottom caps (not shown) similar to those described for the embodiment first described above. The resilient layer 139 can flex together with the interconnect circuit 132 that spans the gap 127. This keeps the contact pads 140, which are exposed on a top surface of the circuit 132, in a planar relationship with each other and thereby facilitates electrical contact with corresponding die contact pads (not shown). The gap 127 and the membrane that overlays it permit surface planarization between the contact pads 140 and the die pads 145, thus reducing the force required to make contact between the two types of pads.

Figures 11, 12A-B and 13A-B show three alternate mechanisms for applying a force to the die/interconnect circuit interface. In Figure 11, the die 422 is placed on the substrate/interconnect circuit assembly 437. A locking collar 459 is secured to the substrate/interconnect circuit assembly 437 inside the I/O pads 436. An oblong locking spring 450 engages a metal piston 461 inserted within the collar 459. The piston 461 compresses a spring and/or elastomer member 428 disposed between the die interface 457 and the piston 461. The piston assembly includes an elastomer 428 and a bottom piece 457 that rests against the die. The piston "snaps" in and out to alternately hold the die in place or allow its removal. Ball seal 480 is part of the locking

collar 459 which provides environmental protection to the die 422 and substrate 437 interface.

Figures 12A and 12B show another alternative carrier 510 in which springs 563 engage fixed top stops 565 and slideable bottom stops 567 and urge the stops apart. The top stops 565 are located in fixed positions on each of four corner posts 569. The bottom stops 567 are disposed at four corners of the carrier substrate and are slideable along the posts 569. The die holder 527 protects the die 522 from rotating when the cap 512 is twisted into position. The springs 563 provide a downward force against the bottom stops 567 which abut against the top cap 512 and push it downward as well.

Figures 13A and 13B show another alternate carrier 610 in which springs 663 are fixedly secured to bottom stops 667 of each of four corner posts 669. The springs 663 are disposed between the bottom stops 667 which move with the posts 669 and fixed top stops 665. The posts 669 are slideable upward and downward. The springs 633 urge the posts 669 downward when the top cap 612 is in place. The die 662 is mounted in a die protector 657. The die protector 657 protects the die from rotating during twist on/off of the cap 612. The springs 663 provide a downward force against the top cap 612.

Figures 14A and 14B explain how the top caps are inserted for both Figures 12A-B and 13A-B. First, the top cap 512/612 is inserted as shown in

Figure 14B. Then it is twisted to the position shown in Figure 14B. In the case of Figures 12A-B, as the twisting takes place, the corners of the top cap 512 engage the underside of the bottom stop 567 and force it toward the top stop 565 (which is fixed) causing compression of the spring 563. In the case of Figures 13A-B, as the twisting takes place, the corners of the top cap 612 engage the underside of the post tops 671 and force them upwards causing compression of the spring 663. In each case, the top cap 512/612 is urged by spring force toward the die/interconnect circuit interface. The amount of force applied to the interface depends upon the compression of the spring.

Various modifications to the preferred embodiment can be made without departing from the spirit and scope of the invention. Thus, the foregoing description is not intended to limit the invention which is described in the appended claims in which:

WHAT IS CLAIMED IS:

1. A bare semiconductor circuit die carrier for use in testing semiconductor circuits, comprising:

a substrate which includes an outer perimeter region;

a multiplicity of I/O pads disposed in the outer perimeter region of said substrate;

an interconnect circuit which includes a composite of a multiplicity of individual electrical conductors which are formed on a polymer dielectric;

wherein said interconnect circuit overlays a top surface of the substrate;

a fence that is sized to receive the die upstands from a portion of the interconnect circuit that is cirsumscribed by the inner perimeter;

a multiplicity of die contact pads disposed on the interconnect circuit within said fence;

wherein said multiplicity of electrical conductors form a multiplicity of electrical paths between said I/O pads and said die contact pads;

wherein a portion of said interconnect circuit circumscribed by said fence includes a compliant region in which a normal force applied to individual die contact pads can planarize said contact pads with respect to each other;

a top cap;

a bottom cap; and

means for securing said substrate and the die between said top cap and said bottom cap with said substrate and the die disposed therebetween.

2. The carrier of claim 1 wherein said at least one polymer dielectric layer provides the compliance in the complaint region.

3. The carrier of claim 1 wherein:

said substrate includes a thinned region beneath said compliant region; and

compliance of the thinned substrate region provides the compliance of the complaint region.

4. A bare semiconductor circuit die carrier for use in testing semiconductor circuits, comprising:

a substrate which includes an inner perimeter which defines an opening and which includes an outer perimeter region;

a multiplicity of I/O pads disposed in the outer perimeter region of said substrate;

an interconnect circuit which includes a composite of a multiplicity of individual electrical conductors which are formed on a polymer dielectric;

wherein said interconnect circuit overlays a top surface of the substrate and extends across the opening;

a fence that is sized to receive the die upstands from a portion of the interconnect circuit that is cirsumscribed by the inner perimeter;

a multiplicity of die contact pads disposed on the interconnect circuit within said fence;

wherein said multiplicity of electrical conductors form a multiplicity of electrical paths between said I/O pads and said die contact pads;

a support member which abuts against a bottom surface of said interconnect circuit;

a top cap;

a bottom cap; and

means for securing said substrate and the die between said top cap and said bottom cap with said substrate and the die disposed therebetween.

5. The carrier of claim 4 wherein:

the defined opening is a center opening; and

said interconnect circuit extends across the opening so as to form a flexible membrane that spans the opening.

6. The carrier of claim 4 further including:

a resilient layer;

wherein a bottom surface of said substrate and a bottom surface of said support member rest upon said resilient layer;

wherein the defined opening is a rectangular gap that circumscribes said support member; and

wherein said interconnect circuit spans the gap.

7. The carrier of claim 4 further including:

a multiplicity of hard particles that protrude from the die contact pads in electrical contact with individual conductors.

8. The carrier of claim 4 further including:

force means for applying a prescribed amount of force to an interface of the die and the interconnect circuit.

9. The carrier of claim 4 further including:

a multiplicity of hard particles that protrude from the die contact pads in electrical contact with individual conductors; and

force means for applying a sufficient amount of force to an interface of the die and said interconnect circuit such that individual particles penetrate any nonconductive material formed on the pads of the die.

10. The carrier of claim 4 wherein said support member is formed from a semiconductor material.

11. A bare semiconductor circuit die carrier for use in testing semiconductor circuits, comprising:

a substrate defining an opening and an outer perimeter;

a multiplicity of I/O pads disposed about the outer perimeter of said substrate;

an interconnect circuit which includes a multiplicity of individual electrical conductors and which overlays a top surface of the substrate and extends across the opening so as to form a flexible membrane that spans the opening;

a multiplicity of die contact pads disposed on the interconnect circuit;

wherein said multiplicity of electrical conductors form a multiplicity of electrical paths between said I/O pads and the die contact pads;

a fence upstanding from the interconnect circuit and sized to receive the die;

a support member which abuts against a bottom surface of said interconnect circuit;

a top cap;

a bottom cap;

means for securing said substrate and the die between said top cap and said bottom cap; and

force means for applying a prescribed amount of force to an interface of the die and said interconnect circuit.

12. The carrier of claim 11 wherein said support member includes a semiconductor support that abuts against the interconnect circuit.

13. The carrier of claim 11 wherein:

said support member includes a semiconductor support that abuts against the interconnect circuit; and

said force means includes a spring.

14. The carrier of claim 11 wherein the interconnect circuit includes a composite of electrical conductors formed on a polymer dielectric.

15. The carrier of claim 11 wherein said electrically conductive particles are positioned on said die contact pads within said fence so as to make electrical contact with pads of the die when the die is received within said fence.

16. The carrier of claim 11 and further including a spacer that abuts said interconnect circuit and said top cap when the top cap is secured to the bottom with said substrate and with the die secured therebetween.

17. The carrier of claim 11 wherein said top cap is formed from metal.

18. The carrier of claim 11 wherein said top cap and said bottom cap are formed from metal.

19. The carrier of claim 11 further including:

a multiplicity of hard particles that protrude from said die contact pads in electrical contact with individual conductors;

wherein said fence is contoured so as to align the die received within said fence such that respective pads of the die directly overlay respective die contact pads; and

wherein said force means applies sufficient force such that individual particles penetrate any nonconductive material formed on the pads of the die.

20. The carrier of claim 19 wherein the multiplicity of particles are electrically conductive.

21. The carrier of claim 11 wherein a layer of polymer dielectric is formed on a top surface of the semiconductor support.

22. The carrier of claim 8 wherein:

said force means includes a spring disposed between said support member and said bottom cap.

23. A bare semiconductor circuit die carrier for use in testing semiconductor circuits, comprising:

a substrate defining an opening and an outer perimeter;

a multiplicity of I/O pads disposed about the outer perimeter of said substrate;

an interconnect circuit which includes a composite of a multiplicity of individual electrical conductors which are formed on a polymer dielectric;

wherein said interconnect circuit overlays a top surface of the substrate and extends across the opening;

a multiplicity of die contact pads disposed on the interconnect circuit which form a multiplicity of electrical paths between said I/O pads and the die contact pads in the flexible membrane;

a multiplicity of electrically conductive particles embedded on the die contact pads in contact with individual conductors;

a fence disposed on the interconnect circuit and contoured so as to align the die such that respective pads of the die directly overlay respective electrically conductive particles that contact the individual conductors;

wherein said fence is defined by a layer of the polymer dielectric which extends from said exposed I/O pads to said fence;

a top cap;

a bottom cap;

a support member that abuts against a bottom surface of said interconnect circuit;

force means for applying a sufficient amount of force to an interface of the die and said interconnect circuit such that individual particles penetrate any nonconductive material formed on the pads of the die;

means for securing said substrate and the die between said top cap and said bottom cap.

24. The carrier of claim 23 wherein:

the defined opening is a center opening; and

said interconnect circuit extends across the opening so as to form a flexible membrane that spans the opening.

25. The carrier of claim 23 further including:

a resilient layer;

wherein a bottom surface of said substrate and a bottom surface of said support member rest upon said resilient layer;

wherein the defined opening is a gap that circumscribes said support member; and

wherein said interconnect circuit spans the gap.

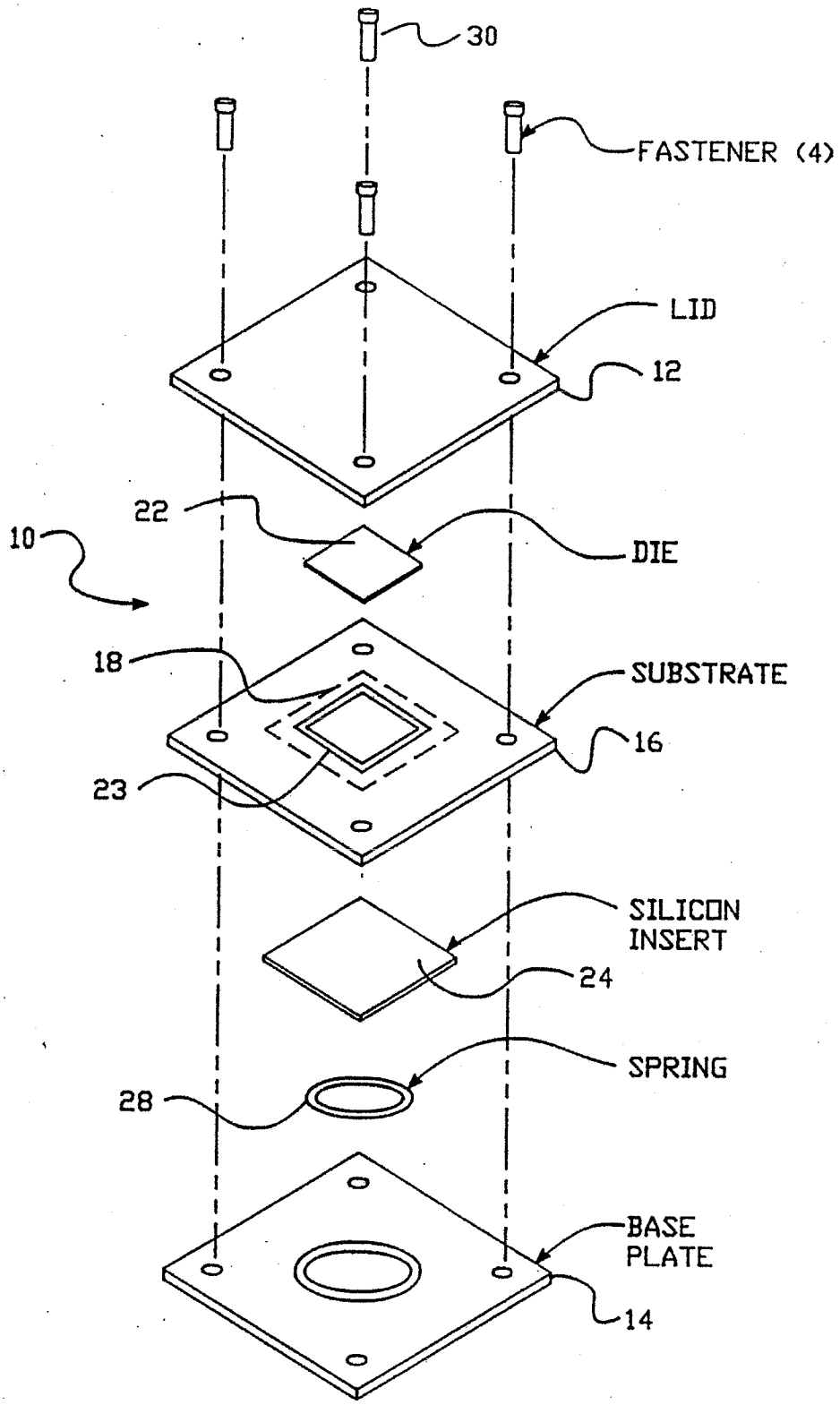
30
FASTENER (4)
LID
12
22
10
DIE
18
SUBSTRATE
16
23
SILICON
INSERT
24
SPRING
28
BASE
PLATE
14

FIG.—1

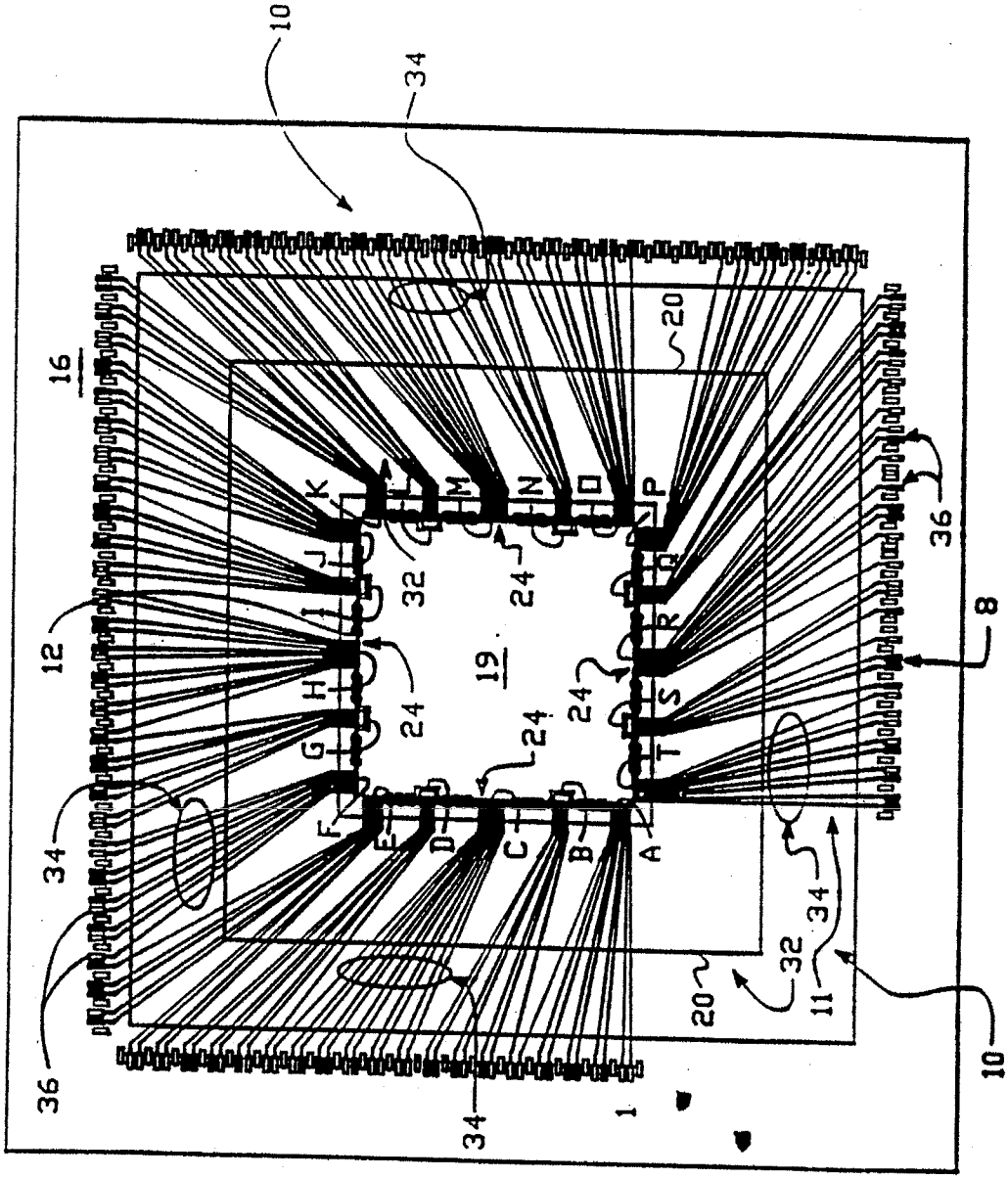

FIG.—2

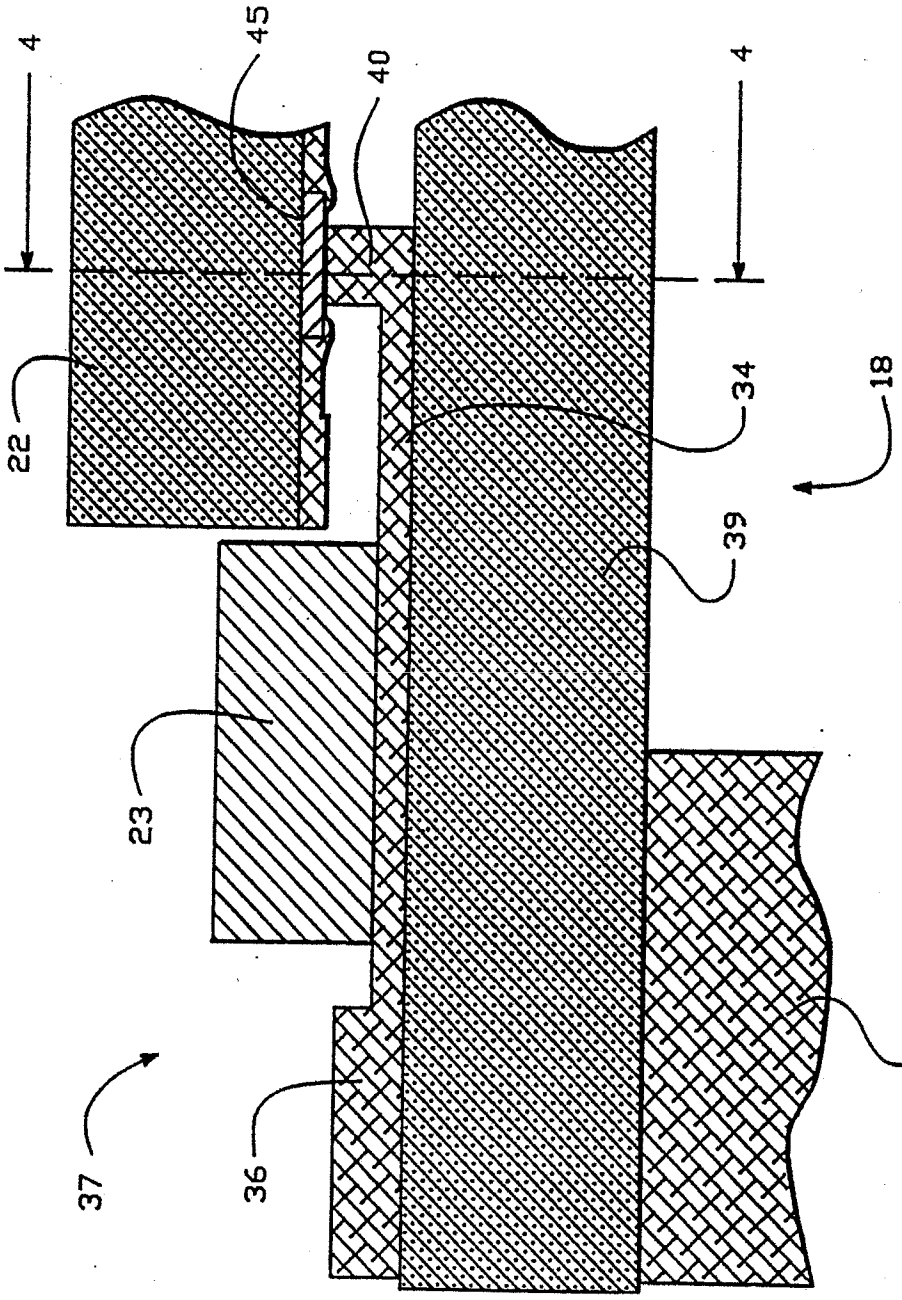

FIG.-3

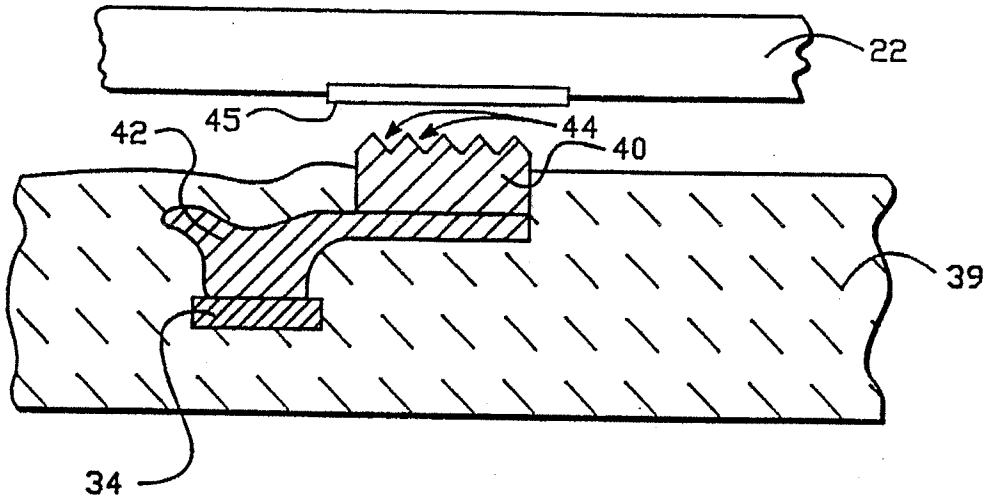

FIG.—4

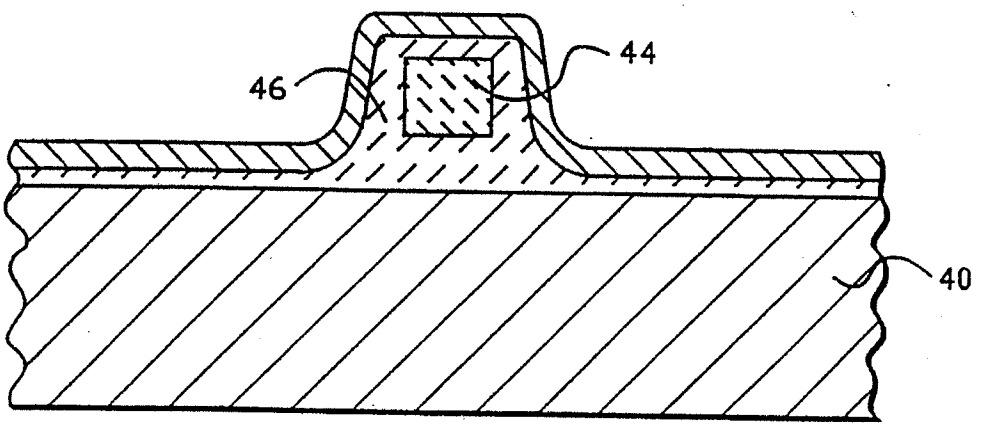

FIG.—5

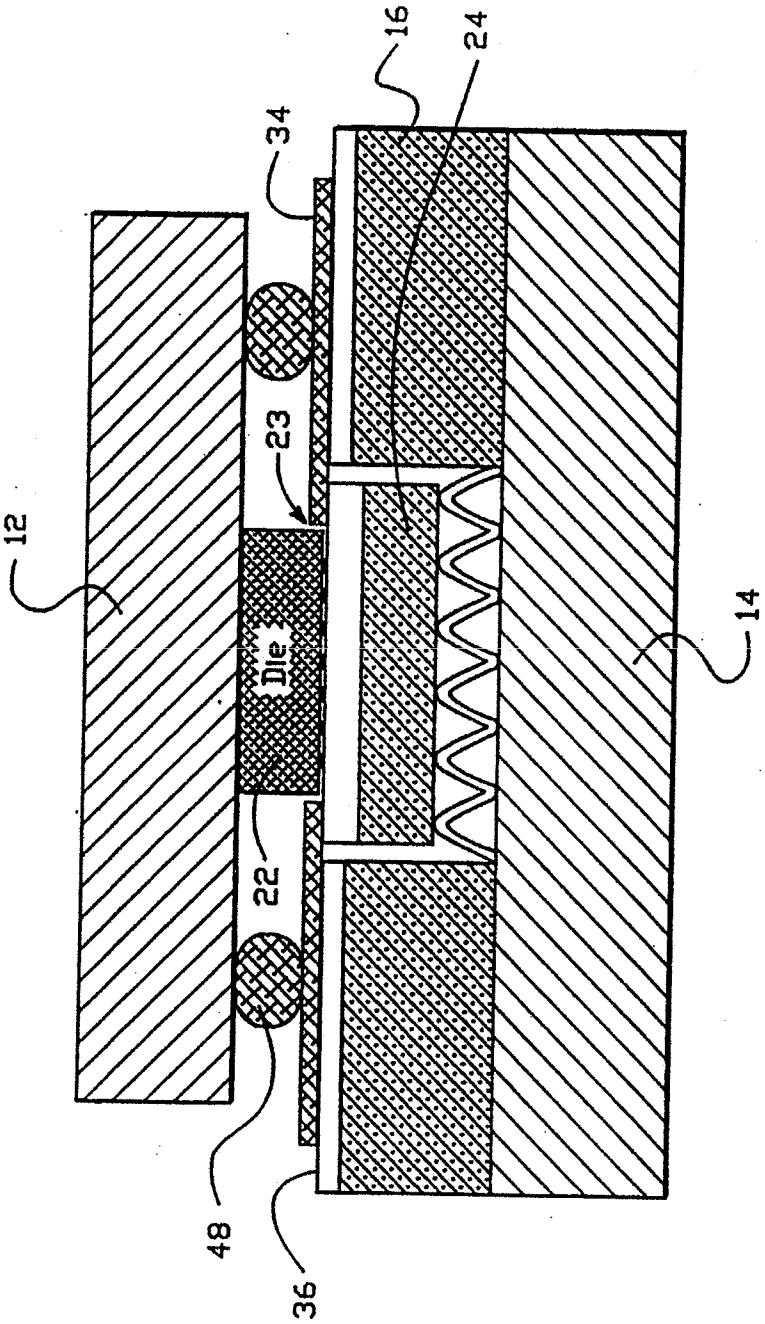

FIG.—6

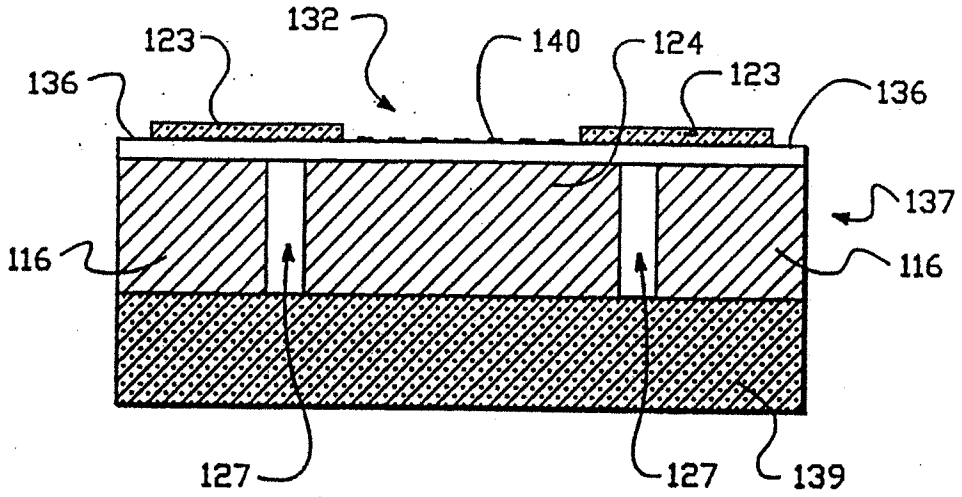
123
132
140
124
123
136
136
137
116
116
127
127
139

FIG.—7A

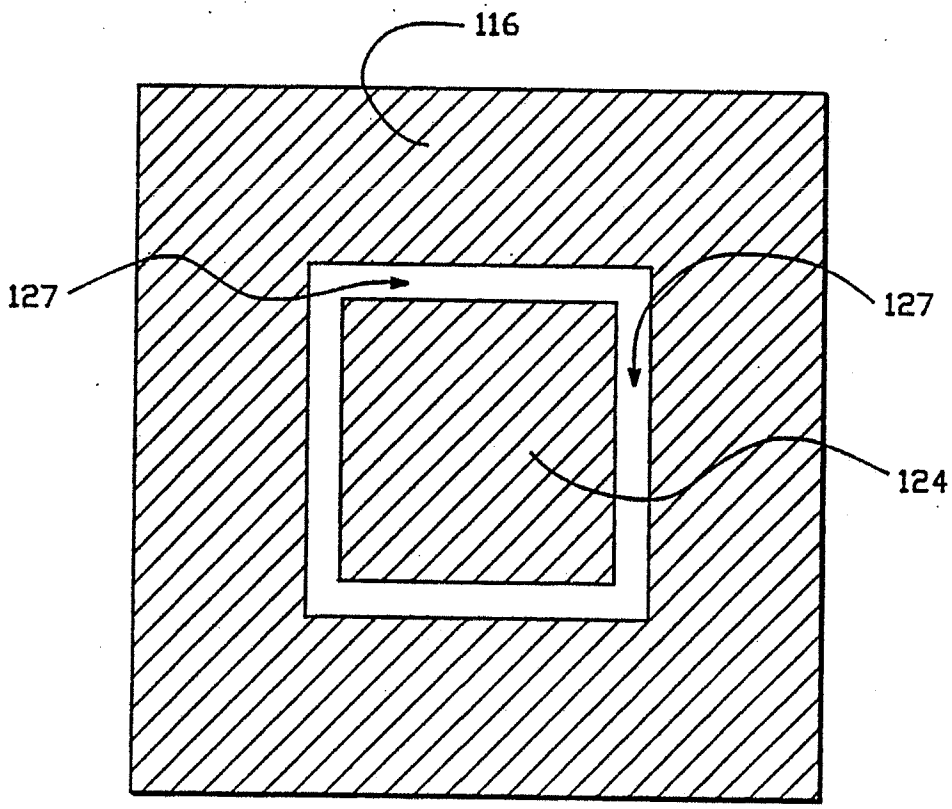
116
127
127
124

FIG.—7B

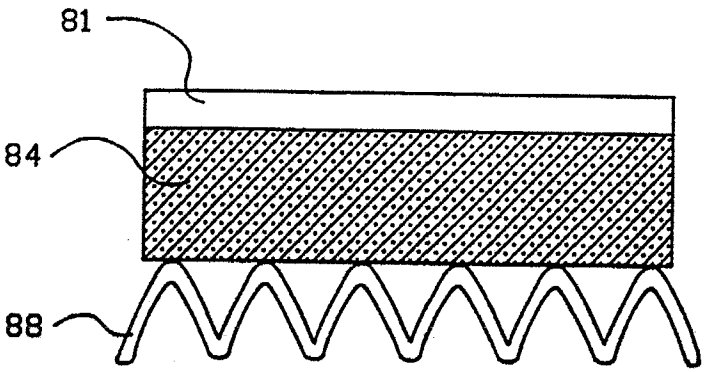

FIG.—8

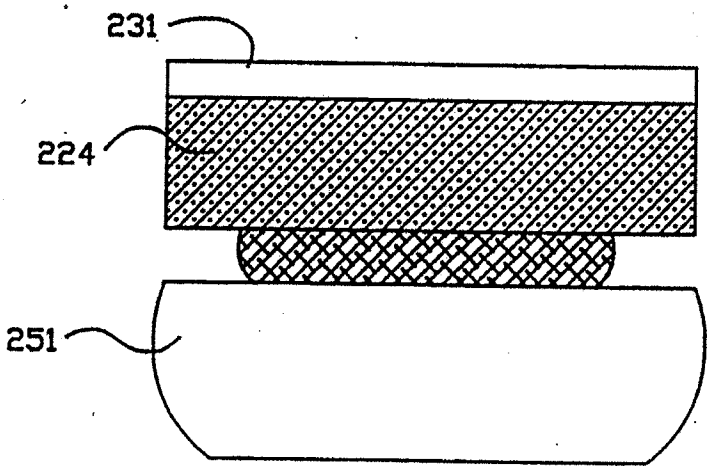

FIG.—9

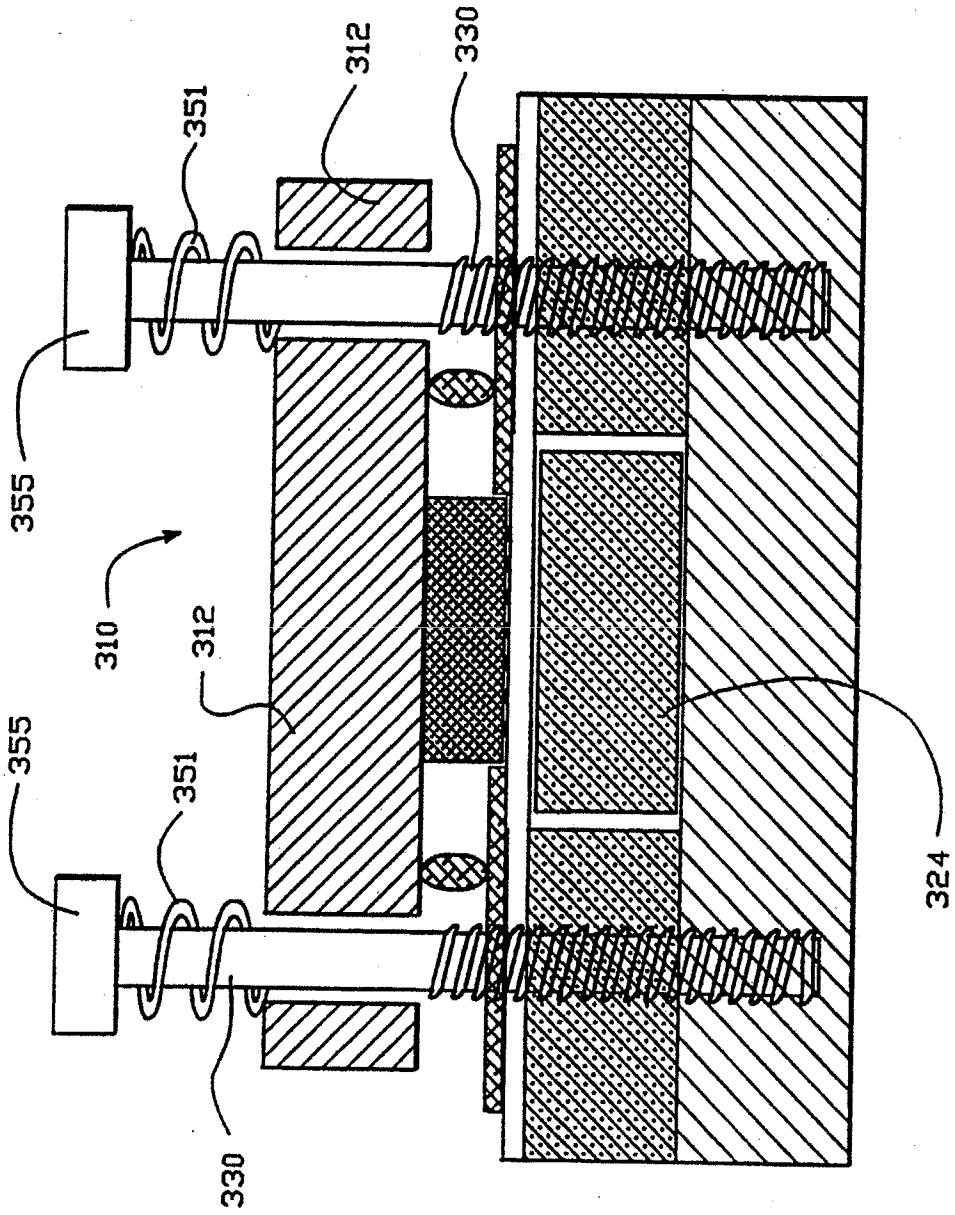

FIG.—10

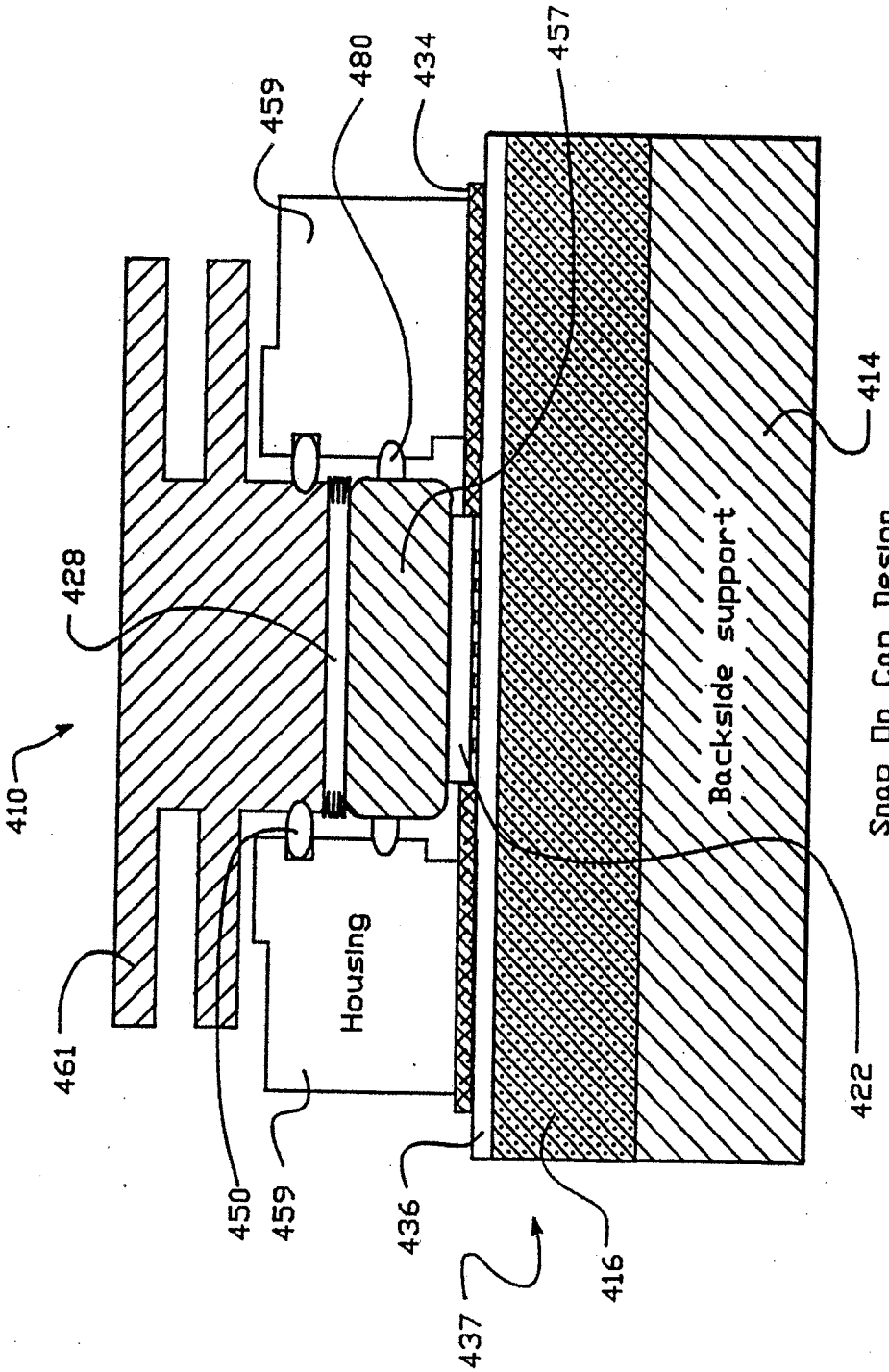
459
480
434
457
414
428
410
Backside support
Snap On Cap Design
Housing
461
450
459
436
437
416
422

FIG.—11

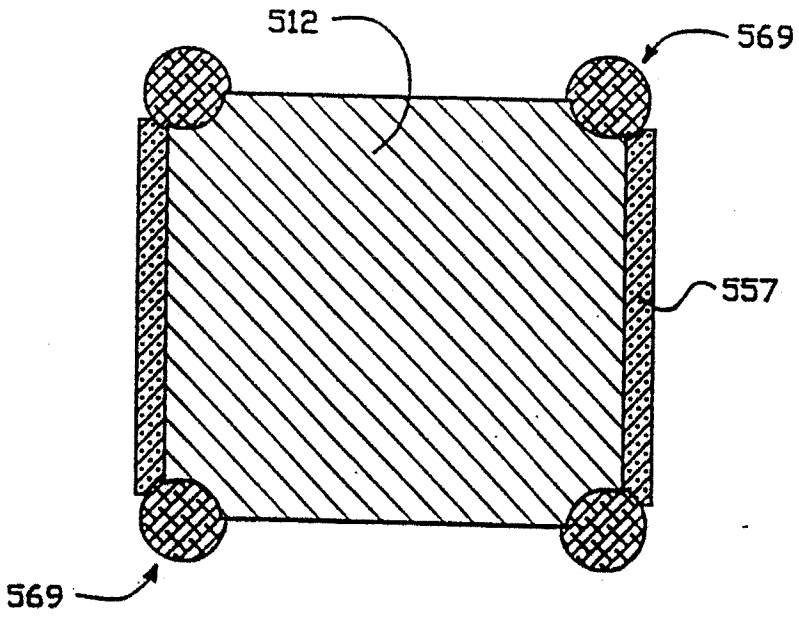

FIG.—12B

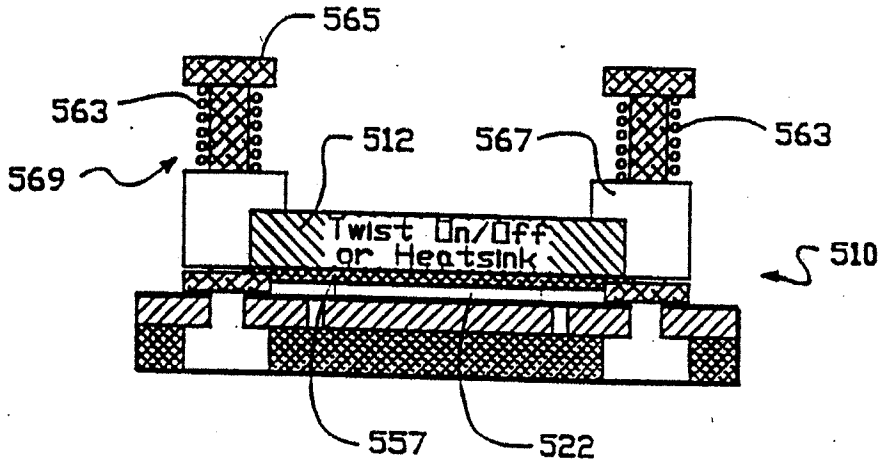

FIG.—12A

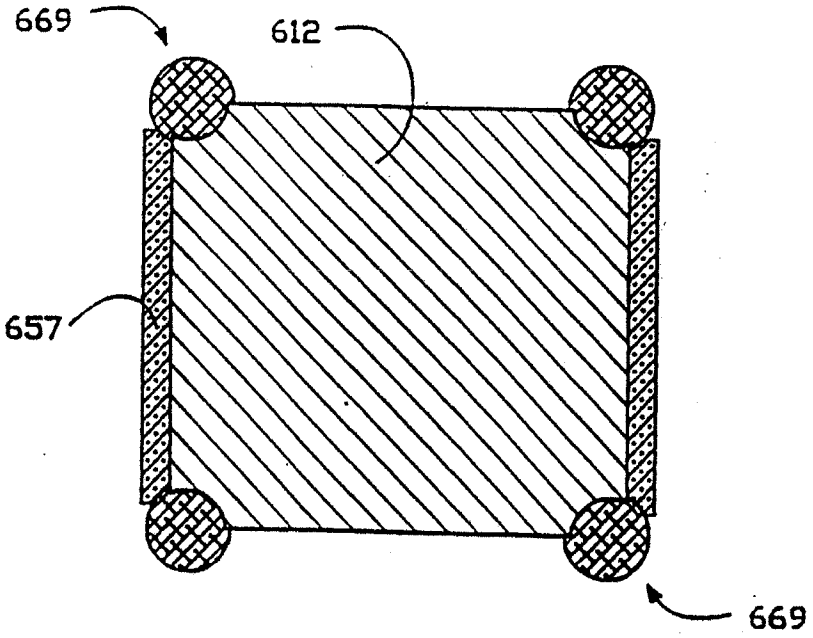

FIG.—13B

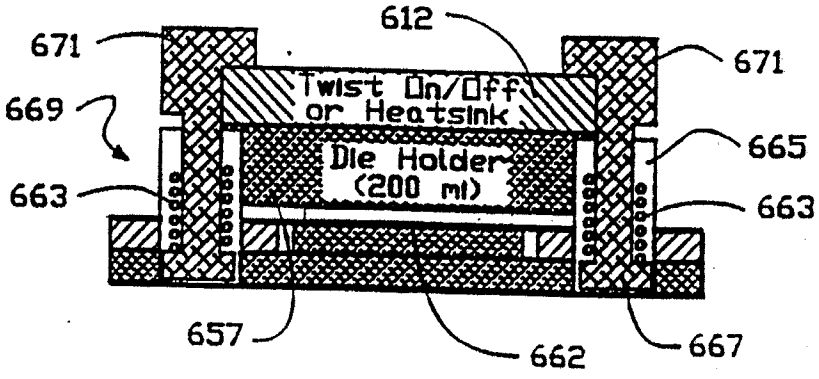

FIG.—13A

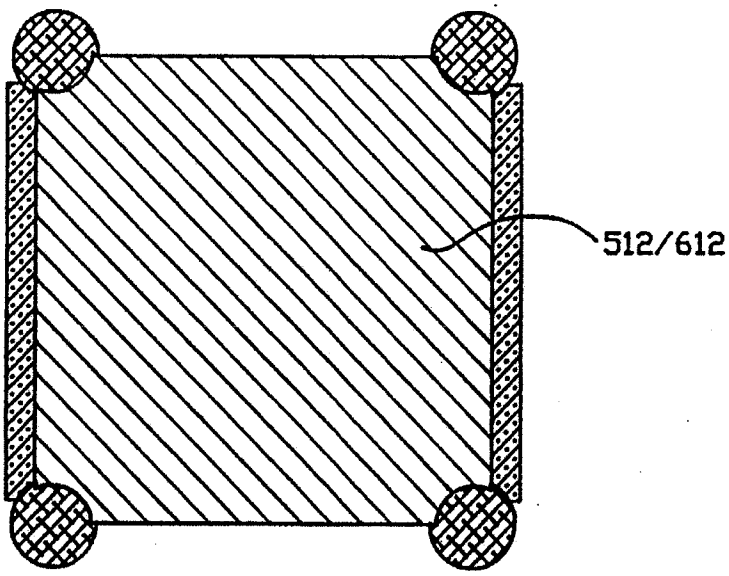

FIG.—14B

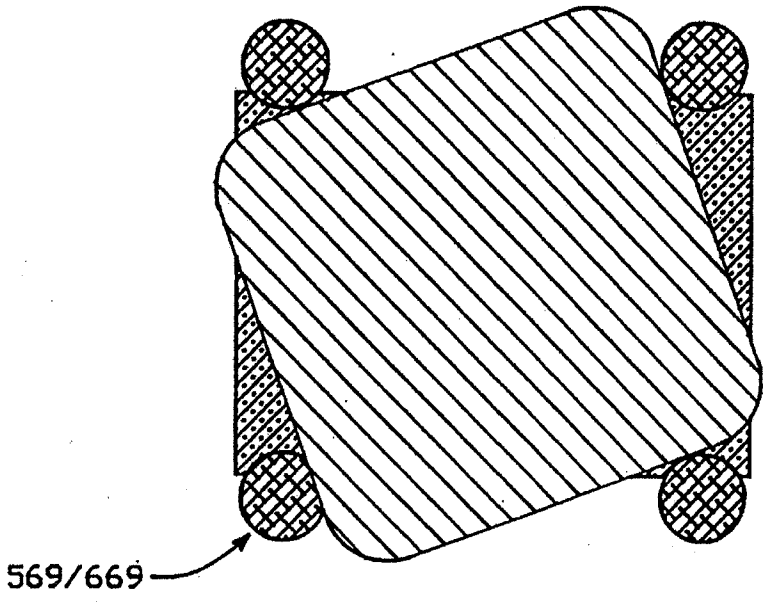

FIG.—14A

INTERNATIONAL SEARCH REPORT

In ational application No.
PCT/US93/11002

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :Please See Extra Sheet.
US CL :324/158F
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 324/158F, 158P, 158R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,782,289 (Schwar et al),1 November 1988, see item 72, figures 2b, 5-6	1-25
Y,P	US, A, 5,176,525 (Nierescher et al), 5 January 1993, see items 236, 246, 236, 206, 526, 528, face figure, figure 6	1-25
Y	US, A, 3,832,632 (Ardezzone et al), 27 August 1974, see abstract	7, 9, 15, 19-20,23
A	US, A, 4,329,642 (Luthi et al), 11 May 1982, see face figure	1-25

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
07 FEBRUARY 1994	MAR 23 1994
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Authorized officer KEN WIEDER
Facsimile No. N.A.	Telephone No. (703) 305-4707

PHI302420

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

In..national application No.
PCT/US93/11002

A. CLASSIFICATION OF SUBJECT MATTER:
IPC (5):

G01R 1/04